

Master Courses

M1: Multiprocessor Systems and Networks on Chip

Organizer: Ahmed Jerraya, TIMA, Grenoble, FR

Speakers: Giovanni De Micheli, Stanford U, US

Sungjoo Yoo, TIMA, Grenoble, FR;

Luciano Lavagno, Politecnico di Torino, IT

Ahmed Jerraya, TIMA, Grenoble, FR

Modern system-on-chip (SoC) design shows a clear trend towards integration of multiple processor cores on a single chip. Typical multiprocessor SoC applications like network processors, multimedia hubs and base-band telecom circuits have particularly tight time-to-market and performance constraints which require a very efficient design cycle. The trend is then to build large designs as a Network-on-Chip. The game is now to interconnect standard components as we used to do for boards a few years ago. This evolution is creating several breaking points in the design process.

This course will address the four main challenges for the design community:

- Prof. Giovanni DeMicheli will consider systems on chips (SoCs) that will be designed and produced in five to ten years from today, with gate lengths in the range 50-100nm. He will talk about the essential problems of interconnect in advanced technologies and the need to address them with a layered methodology that builds upon the experience in networking. He will provide some examples of design practices.
- Dr. Sungjoo Yoo will overview the on-chip communication architecture schemes covering software and hardware parts. The software part includes operating system, device driver, and hardware abstraction layer (HAL). The hardware part may include communication coprocessors such as DMA, bus/network interfaces, communication networks consisting of dynamic/static routers, and memory. He will also explain communication interface architectures such as virtual interface architecture (VIA), intelligent I/O (I2O), etc. in the context of SoC design.
- Prof. Luciano Lavagno will cover the basic concepts of platform-based design, explaining how the separation it offers between users (system designers) and implementers (IP providers) maximises flexibility and re-use, while minimising time to market.
- Dr. Ahmed Jerraya will introduce a component-based design approach to build complex architectures from basic IP modules. The approach provides a natural way to abstract hardware/software interfaces for multiprocessors and network on chip applications. This includes hardware interfaces to adapt components to the communication network and software layer including OS to isolate the software application from the architecture.

M2: Design and Design Methods for RF/Mixed-Signal Integrated Systems

Speakers: Piet Vanassche, KU Leuven, BE
Domine Leenaerts, Philips, NL
Rob Rutenbar, Carnegie Mellon U, US
Walter Daems, KU Leuven, BE
George Papadopoulos, Patras U, GR

Advances in ultra-deep submicron CMOS technology allow the integration on chip of entire systems, including both the digital cores and the analogue interface circuits. The latter provide for the communication or interaction with the outside world. Integrated systems for applications like communications, wireless, consumer, multimedia, biomedical, etc., are therefore increasingly becoming mixed-signal, containing also analogue and/or RF parts. This master course focuses on the design of such RF/mixed-signal systems. The full design flow from system requirements to silicon layout is described, and design methods and tools that support this flow are presented. This is illustrated with several practical design examples, both from existing as well as new emerging wireless applications.

This master course will address the following topics:

- The design flow for RF/mixed-signal systems from system specification to silicon layout will be reviewed and the different design steps will be identified. Architectural front-end exploration methods will be reviewed, and an overview of simulation methods for wireless circuits will be given, including steady-state analysis, phase noise analysis, etc.
- This will then be illustrated with some practical design examples from real-life industrial wireless applications such as Bluetooth and WLAN. The choices for the system architecture will be described, the design of different circuits will be presented, and the design choices and trade-offs that were taken to reduce power and cost will be explained.
- An overview will then be given of existing and emerging design methods and tools that exist to improve the quality and/or increase the productivity in the design of RF/mixed-signal systems. This includes tools for both circuit optimisation and layout synthesis of both mixed-signal and RF blocks, such as VCO's, data converters, etc.
- Finally, the emerging area of ubiquitous, ultra-small, ultra-low-power sensory-based wireless devices with ad-hoc networking capabilities will be described. Examples are body-area sensory networks, security monitoring devices, and so on. Both the radio aspects and the networking aspects will be reviewed and illustrated.