

# Tutorials

## **A1 — Applied Formal Hardware Verification Methods**

Hans Eweking, TU Darmstadt, D

There are now two main areas of successful industrial application of formal verification techniques: (a) the verification of large blocks of combinational circuits which is faster and more efficient than simulation techniques, and (b) the checking of equivalence or of temporal properties of finite state systems. Both types of formal verification rely on the efficient representation of Boolean functions or large state spaces by means of decision diagrams. The tutorial will first give an introduction to various types of decision diagrams (OBDD's, OKFDD's, \*BMD's). Examples of successful applications of decision diagrams to large blocks of combinational circuits will be presented afterwards. The specific problems of using VHDL as input language will be discussed.

Symbolic state space traversal methods allow for the exploration of very large state spaces. The methods can be used to demonstrate the equivalence of two finite state machines or to verify temporal properties by model-checking. In addition, many applications use model-checking as a debugging rather than as a verification tool in order to detect bugs as early as possible and to reduce design time. The tutorial will give an introduction to symbolic state space traversal methods, and will again consider VHDL-related aspects.

## **B1 — Testing Embedded-Core based System Chips**

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Audience: IC designers, test engineers, and their managers, but also (academic) researchers, test methodology developers, and test tool developers.

Abstract: Advances in semiconductor process and design technology enable the design of complex systems-on-chips. Traditional IC design, in which every circuit is designed from scratch and reuse is limited to standard-cell libraries, is more and more replaced by a design style based on embedded large reusable modules, the so-called cores. This core-based design style poses a series of new challenges, especially in the test domain. Therefore, testing of embedded cores is one of the current Hot Topics in the international test community.

This tutorial provides an introduction into core-based design and test, and an overview of current academic and industrial practices in core test. The current status of industry-wide standardization in VSIA and IEEE P1500 is discussed. The main modules of the tutorial are (1) Core-Internal Test Methods, (2) Test Access and Control for Embedded Cores, and (3) Testing Systems-on-Chips.

## **C1 — Towards the Full Integration of CMOS RF Circuits for Wireless Communication**

Michiel Steyaert, KU Leuven, B

For several years the research in the possibilities of CMOS technologies for RF applications has grown enormously. The trend towards deep sub-micron technologies allows the operation frequency of CMOS circuits above 1GHz, which opens the way to integrated CMOS RF circuits. Several research groups have developed high performance down-converters, low phase noise voltage controlled oscillators and dual modulus prescalers in standard CMOS technologies. The research has already demonstrated fully integrated receivers and VCO circuits with no external components, nor tuning or trimming. Further research on low noise amplifiers, up-converters and synthesizers has recently resulted in fully integrated CMOS RF transceivers for DCS-1800 applications. In this tutorial an overview of the trend towards the full integration of front-end circuits in CMOS technologies will be addressed. Some technology limitations, design procedures, analysis tools and RF circuits will be analyzed and discussed in detail.

## **A2— Hardware/Software Co-Design and Java**

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Wayne Wolf, Princeton U, USA

Wolfgang Rosenstiel, U Tuebingen, D

Hardware/Software Codesign has become a strategic technology for modern electronic systems, from VLSI single chips containing embedded cores via boards to large distributed systems made of a heterogeneous network of processors communicating via sophisticated protocols. Codesign is the enabling technology for industry and may also be the bottleneck for faster progress. This tutorial is designed to provide the attendees with a comprehensive background on the state of the arts and the future of codesign.

The tutorial is structured into three parts:

1. Introduction to hardware/software codesign: This part gives the basic concepts underlying codesign and introduces the state of the arts model and techniques used in hardware/software codesign.
2. In-depth study of hardware/software partitioning: Hardware/software co-design techniques require both analysis of design metrics such as performance and area and synthesis algorithms to optimize the design. After introducing the major problems, we will survey techniques for analyzing performance and area, then use those techniques to discuss several different types of co-synthesis algorithms.
3. Future trends, Java for embedded systems: Originally planned for embedded systems, Java became a general purpose wide spread programming language. Recently many new developments revisit Java for its use in the context of embedded systems. This tutorial part will especially concentrate on this subject. Key words are JavaBeans, Embedded Java, Personal Java, Java Card, Jini, Java and real time operating systems, and last but not least Java for simulation and synthesis of hardware.

## **B2— Test and DFT for Practising Engineers**

S. Yadavalli, S. Kundu, S. Sengupta, R. Galivanche, Intel, USA

This tutorial will cover practical aspects of Design For Test (DFT), Automatic Test Pattern Generation (ATPG), and the Manufacturing Test Flow.

Commonly used fault models in the industry: stuck-at, transition and the path delay faults will be reviewed. Realistic fault models for defects such as opens and bridges will also be discussed. Practical ways of extending traditional ATPG tools to address realistic fault models will be presented. The practical aspects of modeling circuits for efficient ATPG and fault simulation will be reviewed in the context of static and dynamic CMOS circuits, as well as memory arrays.

DFT techniques commonly practiced in industry will be reviewed in detail, with emphasis on Built-In Self-Test (BIST) and scan-based DFT schemes. Both logic and memory BIST will be covered along with solutions to related practical problems that enable and enhance coverage using BIST.

The methodology collateral that goes into successful ATPG of a complex design will be discussed. This includes a discussion of scan design rules along with their scope and motivation, techniques and algorithms for selecting scan cells where full scan is not possible, and the impact of violating scan design rules. The roles of related tools such as scan insertion, scan chain reordering and fault diagnosis will be treated.

A typical manufacturing test flow will be described, showing the steps involved in testing a chip from the wafer to the completely packaged stage. The motivation and limitation of each step will be reviewed, and the reason for different measurements at each test step will be discussed. Different types of testers involved at various steps and their capabilities will be presented.

## **C2— Low Power Metrics: From Circuits to Systems**

Joan Figueras, PU Catalunya, ES

The power consumption of CMOS designs is becoming a critical factor to assure portability, reliability and low cost cooling in competitive electronic systems. Metrics to estimate the power in CMOS are aimed to support the power/energy prediction techniques used by the low-power synthesis tools. Adequate models with the right compromise of precision and simplicity are one of the key factors to achieve competitive low power designs.

In this tutorial a bottom up approach to the power estimation problem will be presented. For each topic the state of the art will be surveyed and application examples discussed. Topics dealt with are: Electrical Circuit level power modeling techniques: capacitive switching power, short circuit power, leakage power. Logic Level metrics with special attention to colliding transitions, glitches and hazards. At RTL and System levels the different metrics and techniques for low power design will be discussed and applications presented.

Intended Audience: Design engineers concerned on power/energy consumption. Researchers on design and test of electronic systems with power/energy concerns. Managers with a need to assess future directions of electronic design.